Modelling of source-coupled logic gates

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SUMMARY

In this paper, the modelling of CMOS SCL gates is addressed. The topology both with and without output buffer is treated, and the noise margin as well as propagation delay performance are analytically derived, using standard BSIM3v3 model parameters.

The propagation delay model of a single SCL gate is based on proper linearization of the circuit and the assumption of a single-pole behaviour. To generalize the results obtained to cascaded gates, the effect of the input rise time and the loading effect of an SCL gate are discussed.

The expressions obtained are simple enough to be used for pencil-and-paper evaluations and are helpful from the early design phases, as they relate SCL gates performance to design and process parameters, allowing the designer to gain an intuitive understanding of performance dependence on design parameters and technology.

The model has been validated by comparison with extensive simulations using a 0.35-μm CMOS process. The model agrees well with the simulated results, since in realistic cases the difference is less than 20% both for noise margin and delay. Therefore, the model proposed can be profitably used for pencil-and-paper evaluations and for computer-based timing analysis of complex SCL circuits. Copyright © 2002 John Wiley & Sons, Ltd.

KEY WORDS: SCL gates; modelling; current mode logic gates

1. INTRODUCTION

The demand for high-resolution integrated analog circuits coexisting with digital circuits in the same substrate has recently increased due to the diffusion of digital audio and video signal processing applications, which require high-speed and high-resolution sigma-delta A/D and D/A converters [1–5]. The traditional CMOS static logic has proven to be inadequate for such applications, since it generates a considerable amount of power supply switching noise [5–11], due to the current spikes associated with switching gates. This supply noise couples with the analogue section via substrate coupling or power supply rails, leading to the degradation of resolution [8].

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Even using high-PSRR fully-differential analog circuits and exploiting techniques such as diffusion of guard bands, keeping separate analog and digital supply lines, pads and wires, for high-precision circuits the amount of noise produced by static logic is intolerably high, and other topologies must be used to implement the digital section. Until now, various topologies which require an almost constant supply current have been proposed [11–26], among which the most successful are the source-coupled logic circuits (SCL) [10,14,15,21,26], based on the source-coupled pair of MOS transistors, and their derived versions like FSCL circuits or EF^2SCL [14,26]. Indeed, they allow switching noise to be reduced by two orders of magnitude compared to static CMOS logic [14].

Although various comparisons between static and SCL logic have been carried out in the literature, SCL gates performance has not yet been analytically modelled, neither regarding switching speed, nor static parameters. A model of SCL gates switching speed, measured by propagation delay, is necessary to quickly verify whether the timing constraint is met during the design of a complex SCL circuit, avoiding many computationally expensive circuit simulations. On the other hand, modelling of DC behaviour allows us to verify if the minimum noise immunity required is guaranteed.

In this paper, an analytical approach to modelling SCL gates performance in terms of propagation delay and DC behaviour is developed, and it is then applied to SCL inverters both with and without output buffers. More specifically, the propagation delay and DC parameters (i.e. noise margin, voltage gain and logic swing) are expressed as a function of design and process parameters, which can easily be extracted from standard BSIM3v3 models. Moreover, the delay model is based on the assumption of single-pole behaviour for the SCL transient response, and on a suitable linearization of transistor parameters.

The closed-form expressions obtained relate performance to design parameters in a simple manner, and hence they are also helpful to design at the transistor level of SCL gates. To test the accuracy of the model proposed, we made extensive comparisons with simulations obtained over a large range of load and design conditions, using a 0.35-µm CMOS process. The error exhibited by the delay model is within 35%, while that of the noise margin, voltage gain and logic swing is within 25%, and the typical values are much lower. Thus, the model can also be used for computer-based logic synthesis of complex digital circuits to meet a given speed constraint, while guaranteeing an adequate noise immunity.

Modelling SCL gates without output buffer and its validation is dealt with in Section 2, where the effects of input waveform rise time on the propagation delay and gate input capacitance are also considered. In Section 3 the model is extended to the case with output buffer and then validated. Conclusions are reported in Section 4.

2. MODELLING OF SCL GATES

SCL gates are based on the source-coupled pair of NMOS transistors, which implements a voltage-controlled current switch. The bias current, $I_B$, is steered to one of the two output branches by a network made up of source-coupled pairs, which are driven by the associated differential inputs. The current steered is converted to a differential voltage by an active load implemented by a PMOS transistor working in the linear region. The low switching noise feature of SCL circuits is obtained since the supply current required by the gate is almost constant, which in turn leads to static power dissipation.
In particular, let us consider the SCL inverter in Figure 1, in which the loading effect of the following gates and the wiring capacitance are accounted for by capacitance $C_L$. The NMOS source-coupled pair M1–M2, whose transistors work in the saturation or the cut-off region, is driven by the differential input signal $v_i = v_{i1} - v_{i2}$, and is biased by the constant current source $I_B$, implemented by a current mirror. When $v_i$ is high, the bias current flows through transistors M1 and M3, and the differential output voltage $v_o = v_{o1} - v_{o2}$ is at the low level equal to $v_o = -\Delta V$, where $\Delta V$ is the voltage drop of M3 when its drain current is equal to $I_B$. Analogously, if $v_i$ is low we get $v_o = \Delta V$, hence the logic swing of the gate is equal to $2\Delta V$. To keep M1 out of the linear region, $\Delta V$ must be kept lower than the NMOS threshold voltage, $V_{T,n}$.

### 2.1. Modelling of DC parameters

The static behaviour of a gate is described by three parameters, the logic swing $V_{SWING}$, the voltage gain around the threshold voltage, $A_V$, and the noise margin, NM. The logic swing, as explained before, is equal to $2\Delta V$. Evaluation of $\Delta V$ can be carried out by replacing the PMOS transistor with an equivalent linear resistance, $R_D$.

To evaluate resistance $R_D$, we consider the expression of the drain current, $i_D$, of a PMOS transistor working in the triode region used in the BSIM3v3 MOSFET model, which represents the standard model for deep submicron CMOS technologies [27]:

$$i_D = \frac{I_{DSAT0}}{1 + R_D(I_{DSAT0}/V_{SD})}$$

(1)

where the parameter $R_D = (R_{DSW} E^6 - 6)/W_{eff}$ depends on the empiric model parameter $R_{DSW}$, which accounts for source/drain parasitic resistance, and heavily affects the I–V relationship in today’s CMOS processes with lightly doped drain (LDD). It is worth noting that $R_D$ does not represent a physical resistor, but only a corrective factor. As demonstrated in Appendix A, the ratio $I_{DSAT0}/V_{SD}$ is equal to $1/R_{int}$, where

$$R_{int} = \left[\mu_{eff,p} C_{OX} \frac{W_{eff,p}}{L_{eff,p}} (V_{DD} - |V_{T,p}|)\right]^{-1}$$

(2)
which represents the ‘intrinsic’ resistance of the PMOS transistor in the triode region (i.e. it does not account for the parasitic drain/source resistance). The term \( \mu_{\text{eff},p} \) represents the effective hole mobility (A2) defined in Appendix A, parameters \( W_{\text{eff},p} \) and \( L_{\text{eff},p} \) are the effective channel width and length, \( C_{\text{OX}} \) is the oxide capacitance per area, and \( V_{T,p} \) is the threshold voltage.

To simplify the expression of \( i_D \), we expand Equation (1) in Taylor series truncated at the first-order term

\[
i_D = I_{\text{DSAT0}} \left( 1 - \frac{R_{DS}}{R_{\text{int}}} \right)
\]

From Equation (3), the equivalent resistance of the PMOS transistors \( R_D = V_{SD}/i_D \) results as

\[
R_D = \frac{R_{\text{int}}}{1 + R_{DS}/R_{\text{int}}}
\]

By inspection of Equations (2) and (4), the equivalent resistance \( R_D \) of the PMOS load transistors depends on their aspect ratio and process parameters. Using Equation (4), we get

\[
\frac{V_{\text{SWING}}}{V_{DD}} = 2R_D I_B,
\]

The threshold voltage of the gate in Figure 1 is equal to zero, due to the symmetry of the circuit, and the associated voltage gain around this bias point is equal to \( g_{m,n} R_D \), where \( g_{m,n} \) is the small-signal transconductance of transistors M1–M2 with \( I_{D1,2} = I_B/2 \).

Transconductance \( g_{m,n} \) for short-channel transistors is evaluated using the well-known expression

\[
\sqrt{2} \frac{\mu_{0,n} C_{\text{OX}} W_{\text{eff},n} / L_{\text{eff},n} (I_B/2)}{V_{\text{DS}}} \]

valid for long channel devices, and replacing the long channel mobility, \( \mu_{0,n} \), in it with an effective electron mobility, \( \mu_{\text{eff},n} \), given by Equation (A2). Assuming that \( V_{\text{GS}} \) of M1 and M2 is small enough to neglect mobility degradation, relationship (A2) for NMOS is simplified into

\[
\mu_{\text{eff},n} = \mu_{0,n} / \left( 1 + V_{\text{DS}} / E_{\text{SAT},n} / L_{\text{eff},n} \right),
\]

whose value depends on the model parameter \( E_{\text{SAT},n} \), the effective channel length \( L_{\text{eff},n} \) and the bias value of \( V_{\text{DS}} \). Since \( v_1 = v_2 = v_{\text{o1}} = v_{\text{o2}} = V_{\text{DD}} - \Delta V/2 \) and \( I_{D1,2} = I_B/2 \) when the gate is biased around the logic threshold, voltage \( V_{\text{DS}} \) of transistors M1–M2 is equal to their \( V_{\text{GS}} \), which can be underestimated to \( V_{T,n} \) for the sake of simplicity (i.e. set \( V_{\text{DS}} \approx V_{T,n} \) in \( \mu_{\text{eff},n} \)).

Substituting \( \Delta V = R_D I_B \), the resulting expression of the voltage gain \( A_V \) is

\[
A_V = \Delta V \sqrt{\frac{\mu_{0,n} C_{\text{OX}}}{1 + V_{T,n} / E_{\text{SAT},n} / L_{\text{eff},n}} \frac{W_{\text{eff},n}}{L_{\text{eff},n}} \frac{1}{I_B}}
\]

The evaluation of the noise margin, NM, can be obtained after simple calculations, developed in Appendix B, which lead to the following expression:

\[
\text{NM} = \Delta V \left( 1 - \frac{\sqrt{2}}{A_V} \sqrt{1 - \frac{1}{\sqrt{2} A_V}} \right) \approx \Delta V \left( 1 - \frac{\sqrt{2}}{A_V} \right)
\]

By inspection of Equation (7), the noise margin of an SCL gate is proportional to the logic swing, and roughly equal to it if \( A_V \) is in the order of 4–5.
2.2. Validation of the model of DC parameters

The parameters modelled in the previous subsection were compared to simulation results obtained for an SCL inverter, using a 0.35-μm CMOS process, whose main parameters are summarized in Table I. To this end, several DC simulations were performed with $V_{DD} = 3.3\, \text{V}$, $I_B$ ranging from 5 to 100 μA, choosing the transistors aspect ratio to get $A_V$ ranging from 2 to 7, and $\Delta V$ from 200 to 900 mV (i.e. a maximum value slightly lower than $V_{T,n}$ under body effect).

The simulated and predicted results are plotted in Figures 2(a), 2(b) and 2(c), in which the scattering plots of the logic swing, $V_{SWING}$, the magnitude of voltage gain, $A_V$, and the resulting noise margin, NM, are, respectively, reported. From Figures 2(a)–2(c), it is evident that the predicted values are close to the simulated ones. More specifically, the maximum error between the model results and the simulated ones for $V_{SWING}$, $A_V$ and NM is equal to 24.7, 25.9 and 24.7%, respectively, and in typical cases the error is significantly lower, as can be deduced from the average and standard deviation values of the error reported in Table II. It is worth noting that the model always underestimates $V_{SWING}$ and overestimates $A_V$.

2.3. Modelling of propagation delay with a step input waveform

The transient behaviour of an SCL gate is well described by its propagation delay, $\tau_{PD,SCL}$. Since it depends on the input signal waveform [6], we first analyse the case with a step input waveform in this subsection, and then the results will be extended to more general cases in the next one.

To model the propagation delay of the SCL inverter in Figure 1, it is worth noting that the NMOS transistors work in the saturation region for most of the time, and their source voltage is the same for both input logic values, since it is fixed by the NMOS transistor in the ON state. Thus, linearizing the circuit around the bias point with $v_i = 0$, the half-circuit concept applies, since the circuit is symmetrical and input is differential.

The equivalent linear half circuit obtained is shown in Figure 3, where transistor M1 (M2) is represented by its small-signal model, transistor M3 (M4) is linearized as an equivalent resistance $R_D$, and subscripts n and p refer to NMOS and PMOS devices, respectively. The capacitive effects associated with the PMOS and NMOS transistors consist of $C_{db}$, which represents the drain–bulk junction capacitance, and $C_{gd}$, which schematizes the channel and the overlap contribution between gate and drain.
Figure 2. (a) Scattering plot of predicted values versus simulated values of the logic swing. (b) Scattering plot of predicted values versus simulated values of the magnitude of the voltage gain. (c) Scattering plot of predicted values versus simulated values of the noise margin.

The network in Figure 3 is a first-order circuit with a time constant $\tau$ that can be evaluated by applying the open-circuit time constant method, and the resulting delay is $0.69\tau$, if a step input waveform is applied. Hence, the propagation delay $\tau_{PD,SCL}$ of the SCL gate

$\tau$The high-frequency zero was neglected; its effect on the transient behaviour of the gate is a small initial overshoot during switching.
Figure 3. Equivalent linear circuit of the SCL inverter in Figure 1.

Table II.

<table>
<thead>
<tr>
<th></th>
<th>Maximum (%)</th>
<th>Average (%)</th>
<th>Standard deviation (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{SWING}}$</td>
<td>24.7</td>
<td>14.7</td>
<td>5</td>
</tr>
<tr>
<td>$A_V$</td>
<td>25.9</td>
<td>12.9</td>
<td>4</td>
</tr>
<tr>
<td>NM</td>
<td>24.7</td>
<td>7.6</td>
<td>5.7</td>
</tr>
</tbody>
</table>

The expression obtained is simple and, hence, it can be profitably used in pencil-and-paper calculations. Moreover, relationship (8) shows how delay depends on design and process parameters and allows the designer to get the necessary intuitive insight into the circuit behaviour.

The capacitances in Equation (8) are obtained through proper linearization of the original circuit, and their dependence on bias current, transistor aspect ratio and process parameters must be specified. The NMOS capacitances $C_{gd,n}$ and $C_{db,n}$ are those in the saturation region, thus the former is roughly equal to the overlap capacitance between the gate and the drain, equal to $C_{gd0}W_{\text{eff}}$ ($C_{gd0}$ is a model parameter which represents the overlap gate–drain capacitance per unit channel width); since voltages move rapidly over a wide range, the latter is evaluated by modifying its value in a zero-bias condition via coefficients $K_j$ given by [6]

$$K_j = \frac{\phi^m}{V_2 - V_1} \left[ \frac{(\phi - V_1)^{1-m}}{1-m} - \frac{(\phi - V_2)^{1-m}}{1-m} \right]$$

where $\phi$ is the built-in potential across the junction, $m$ is the grading coefficient of the junction, and $V_1$ and $V_2$ are the minimum and maximum direct voltages across the junction, respectively. The drain–bulk PMOS capacitance $C_{db,p}$ can be evaluated in the same way as for $C_{db,n}$.

Capacitance $C_{gd,p}$ is equal to the sum of the overlap contribution, given by $C_{gd0}W_{\text{eff},p}$, and the intrinsic contribution associated with the channel charge of the PMOS transistors working in the triode region, $C_{gd,p,\text{int}}$. Unfortunately, the evaluation of $C_{gd,p,\text{int}}$ in the linear region cannot be carried out in the same manner as for long-channel devices, since the decomposition of channel capacitance into gate–source and gate–drain capacitances no longer
applies in submicron technologies [27,29,30]. In the BSIM3v3 capacitance model [27], the
channel charge transfer is modelled by transcapacitances $C_{ij}$, defined as

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

(10)

where $Q_i$ is the charge associated with the MOSFET terminal $i$, and $V_j$ is the voltage of the
terminal $j$. The contribution $C_{gd,p,int}$ accounts for the variations in the drain charge $Q_D$
due to the drain–gate voltage, and it can thus be expressed as a capacitance equal to $C_{dd}$, since
the gate, source, and bulk voltages of transistors M3–M4 are fixed.

To evaluate $C_{dd}$, let us consider the expression of $Q_D$ in the strong inversion:

$$Q_D = -W_{\text{eff}}L_{\text{eff}}C_{\text{OX}}\left[\frac{V_{SG} - |V_T|}{2} - \frac{3A_{\text{bulk}}V_{SD}}{4} + \frac{(A_{\text{bulk}}V_{SD})^2}{8(V_{SG} - |V_T| - A_{\text{bulk}}/2V_{SD})}\right]$$

$$\cong -W_{\text{eff}}L_{\text{eff}}C_{\text{OX}}\left[\frac{V_{SG} - |V_T|}{2} - \frac{3A_{\text{bulk}}V_{SD}}{4}\right]$$

(11)

where parameter $A_{\text{bulk}}$ can be approximated to its maximum value $A_{\text{bulk, max}}$ that is slightly
greater than unity, as shown in Appendix A, and $V_{SD} \ll (V_{SG} - |V_T|)/A_{\text{bulk}}$ was assumed. Dif-
ferentiating Equation (11) with respect to $V_D$ and approximating $A_{\text{bulk}}$ to its maximum value
$A_{\text{bulk, max}}$, we get

$$C_{dd} = \frac{3}{4} A_{\text{bulk, max}} W_{\text{eff}}L_{\text{eff}}C_{\text{OX}}$$

(12)

From Equation (12) it is evident that using the expression valid for long-channel devices (i.e.
$C_{gd,p,int} = \frac{1}{2} W_{\text{eff},p}L_{\text{eff},p}C_{\text{OX}}$) leads to unacceptable errors.

2.4. Validation of the propagation delay model and effect of the non-zero input signal
rise time

To check the validity of the delay model, the results obtained with Equation (8) were com-
pared to simulation results with a step input waveform under a variety of design and load
conditions, using the 0.35 µm CMOS process described above. The bias current was var-
ied from 5 to 100 µA, the transistors aspect ratios were sized to obtain the typical values
$V_{\text{SWING}} = 700$ mV and $A_V = 3$, and the load capacitance, $C_L$, was set to 0 F, 50 fF, 200 fF and
1 pF.

In Figures 4(a), 4(b), 4(c) and 4(d) the simulated delay and that predicted by Equation
(8) are plotted versus the bias current, $I_B$, for a load capacitance equal to 0 F, 50 fF, 200 fF and
1 pF, respectively. As expected, delay is decreased by increasing the bias current, $I_B$, and
asymptotically tends to a constant value.

The model is in agreement with simulated results, as is shown in Figure 5, that reports
the model error with respect to Spectre simulations versus $I_B$, for a load capacitance equal
to 0 F, 50 fF, 200 fF and 1 pF. The maximum error in actual cases (i.e. with non-zero load
capacitance) is equal to 15%, and it is as high as 19% in the non-realistic case with $C_L = 0$ F.
Therefore, the model is sufficiently accurate to be used in pencil-and-paper calculations and
automatic gate-level timing analysis. To get an idea about reasonable values used in practical
Figure 4. (a) Simulated and theoretical delay versus bias current, $I_B$, with $C_L = 0 \text{ F}$. (b) Simulated and theoretical delay versus bias current, $I_B$, with $C_L = 50 \text{ fF}$. (c) Simulated and theoretical delay versus bias current, $I_B$, with $C_L = 200 \text{ fF}$. (d) Simulated and theoretical delay versus bias current, $I_B$, with $C_L = 1 \text{ pF}$.

Figure 5. Error of Equation (15) with respect to simulated results versus bias current, $I_B$.

cases, consider an SCL gate with $I_B = 20 \mu\text{A}$, $C_L = 50 \text{ fF}$, $(W/L)_n = 8/0.3$, $(W/L)_p = 0.6/0.7$ and $V_{DD} = 3.3 \text{ V}$. The predicted and simulated delay are, respectively, equal to 620 and 730 ps, and differ by 15%.

The results presented until now are based on the assumption that the input waveform of the considered gate is an ideal step. Applying actual input waveforms, it is expected that the value of the delay changes. To quantify this variation, we evaluated the delay of a single SCL gate with a load capacitance equal to 0 F, 50 fF, 100 fF, 200 fF, 400 fF and 1 pF, and a
bias current ranging from 5 to 100 μA. The considered gate was driven by a realistic input waveform, obtained from the output voltage of either a single SCL gate or a chain made up of two to four SCL gates. Thus, a very wide range of conditions was considered, including the cases with an input waveform much faster or slower than the output waveform by up to two orders of magnitude.

The results obtained are collected in the scattering plot of Figure 6, where we report the step input delay of the considered SCL gate on the x-axis and the actual delay on the y-axis. Analysis of Figure 6 reveals that the actual delay is close to that with a step input. More specifically, the difference between the two delay values is always lower than 24%, and is typically much lower, since its average value is 6.8%. This means that the delay of an SCL gate is not very sensitive to the input waveform, in contrast to an ideal first-order circuit behaviour. Hence, once again, relationship (8) obtained for the special case of a step input well approximates the delay for actual input waveforms.

2.5. Cascaded gates and loading effects associated with SCL gates

In the derivation of Equation (8), we considered a single SCL gate driving an equivalent load capacitance, $C_L$, that models the wiring capacitances and the input capacitances associated with the following gates. In order to evaluate the delay of cascaded gates, it is necessary to know the input capacitance $C_{\text{input}}$ of each gate to evaluate the delay of the previous one.

As highlighted in Section 2.2, the source voltage of transistors M1–M2 in Figure 1 has the same value, regardless of the logic input value. Hence, the input capacitance $C_{\text{input}}$ seen from

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As an example, for very slow input waveforms a linear first-order circuit would exhibit a delay roughly equal to the circuit time constant, $\tau$ which differs from the step input value $0.69\tau$.

---

the gate of M1 (or M2) is equal to its gate–source capacitance evaluated in the saturation region, roughly equal to

$$C_{\text{input}} = \frac{2}{3} W_{\text{eff}, n} L_{\text{eff}, n} C_{\text{OX}}$$

(13)

The accuracy of this expression was tested by comparison with simulations. In particular, we evaluated the delay of several SCL gates with different size and bias current, loaded by another gate, whose input capacitance was the object of the analysis. From simulations, we evaluated the equivalent input capacitance of the driven gate as the linear capacitance that, when substituted to this gate, leads to the same delay of the driving gate. The difference obtained between the simulated equivalent input capacitance and the theoretical value was always lower than 15%, and typically lower than 10%. Hence, the expression of $C_{\text{input}}$ is sufficiently accurate for practical purposes.

3. MODELLING OF SCL GATES WITH OUTPUT BUFFER

To improve the driving capability of the gate and therefore its switching speed, or to shift the common-mode value of the output nodes voltage, an output buffer can be added to each output node, as shown in Figure 7, where $v_o = v_{o1} - v_{o2}$ is the differential output voltage of the gate, and $v_{i_{\text{buf1}}}$ and $v_{i_{\text{buf2}}}$ are the input voltages of the two buffers, respectively. The output buffer is a source-follower stage biased by the current source $I_{\text{SF}}$. In the following we deal with the modelling of the DC parameters and the delay of SCL gates with output buffers.

The static parameters $V_{\text{SWING}}$, $A_V$ and NM of the SCL inverter in Figure 7 can be derived by properly modifying the results obtained in the previous section. Indeed, the small-signal gain of the common-drain stage (i.e. the ratio $v_o/(v_{i_{\text{buf1}}} - v_{i_{\text{buf2}}})$) is equal to [32]

$$\frac{v_o}{v_{i_{\text{buf1}}} - v_{i_{\text{buf2}}}} = \frac{1}{1 + g_{m_{\text{buf}}} / g_{m_{\text{buf}}}}$$

(14)
where $g_{mb, buf}$ and $g_{m, buf}$ are, respectively, the body effect transconductance and the transistor transconductance, and their ratio is almost constant and close to unity. Thus, the voltage gain, $A_V$, the logic swing, $V_{SWING}$, and the noise margin, NM, are almost equal to those of the SCL gate without the output buffer.

Predicted values of $V_{SWING}$, $A_V$ and NM were compared to simulation results, in the same conditions as in Section 2.2, with $I_{SF}$ ranging from 5 to 100 $\mu$A, and setting the buffer transistors aspect ratio equal to 0.6/0.3, 3/0.3 and 6/0.3. Simulations reveal that the logic swing and the voltage gain agree with the model and the error is due only to the internal SCL gates.

The propagation delay of an SCL gate with the output buffer in Figure 7, $\tau_{PD,SCL, buf}$, can be evaluated by applying the methodology described in the previous section, and decomposing the delay into the contribution of the SCL gate $\tau_{PD, SCL}$, and that of the buffer, $\tau_{PD, buf}$:

$$\tau_{PD,SCL,buf} = \tau_{PD,SCL} + \tau_{PD,buf}$$

(15)

The contribution of the internal SCL gate, $\tau_{PD,SCL}$, is given by Equation (8), in which $C_L$ must be set to zero, while that of the buffer, $\tau_{PD,buf}$, is evaluated by driving the source-follower stage with the Thevenin equivalent circuit seen at the output of the internal SCL gate, modeled with a voltage source $V_{th}$ and a resistance $R_{th}$. Hence, $\tau_{PD,buf}$ can be evaluated by analyzing the circuit in Figure 8, which depicts the linearized buffer circuit driven by the Thevenin equivalent circuit of the SCL gate.

In Figure 8, capacitances $C_{gd,buf}$ and $C_{gs,buf}$ represent the gate–drain and the gate–source contributions, and are evaluated as small-signal capacitances in the saturation region. Moreover,

*Typical values of $g_{mb, buf}/g_{m, buf}$ range from 0.1 to 0.2; for the 0.35-$\mu$m CMOS process used, we get $g_{mb, buf}/g_{m, buf} \approx 0.13$, leading to $t_{o}(V_{i1, buf1} - V_{i2, buf2}) = 0.88$.

†In the SCL gate output impedance, only the resistive contribution was considered, since the output capacitance does not contribute to the delay. This can be shown by considering the effect of the output capacitance of SCL gate, $C_{out}$, on the transfer function of the circuit in Figure 8, which can be approximated with a first-order numerator $(1 + a_1 s)$ and denominator $(1 + b_1 s)$, leading to a delay equal to $0.69(b_1 - a_1)$ [31]. Since considering $C_{out}$ determines an equal increase in $a_1$ and $b_1$ by $R_D C_{out}$, the delay is not affected by $C_{out}$.
the body effect was taken into account because it affects the contribution of capacitance $C_{\text{gs,buf}}$ to the input loop. Indeed, applying the Miller theorem to $C_{\text{gs,buf}}$ and using Equation (14), this contribution results in $C_{\text{gs,buf}}(1 - v_\text{o}/(v_{\text{in,buf1}} - v_{\text{in,buf2}}))$ (where $v_{\text{out1,2}}/v_{\text{L,buf1,2}}$ is given by Equation (14)).

The transconductance of the transistor implementing the buffer, $g_{\text{m,buf}}$, can be evaluated as explained in Section 2.1, provided that in the effective electron mobility ($A_2$) $V_{\text{DS}}$ and $V_{\text{FB}}$ are approximated with their maximum values (i.e. $V_{\text{GS}} + \Delta V$ and $V_{\text{DD}} - V_{\text{GS}}$, respectively), and $V_{\text{GS}}$ is underestimated by $V_{\text{T,n}}$.

The circuit in Figure 8 has a transfer function with two poles and one high-frequency zero, that exhibits a dominant-pole behaviour for practical values of $I_B$ and $C_L$ (detailed analysis shows that the second pole is greater than the first at least by one order of magnitude). Therefore, the buffer circuit can be assimilated to a first-order system, whose delay is equal to 0.69 times its time constant. Applying the time constant method, we get the following expression of the buffer delay:

$$
\tau_{\text{PD,buf}} = 0.69 \left[ R_D \left( C_{\text{gd,buf}} + C_{\text{gs,buf}} \frac{(g_{\text{mb,buf}}/g_{\text{m,buf}})}{1 + (g_{\text{mb,buf}}/g_{\text{m,buf}})} \right) + \frac{C_L + C_{\text{gs,buf}}}{g_{\text{m,buf}}} \right]
$$

(16)

where the source–bulk capacitance was neglected with respect to $C_L$. From Equation (16), the buffer delay is equal to the sum of two terms, whose circuitual meaning is evident: the first is proportional to $R_D$ and models the loading effect of the buffer on the internal SCL gate, the second is inversely proportional to $g_{\text{m,buf}}$, and hence it depends on the buffer driving capability.

Accuracy of Equations (15) and (16) was tested by extensive Spectre simulations using the 0.35 $\mu$m CMOS process described above, with bias current $I_{\text{SF}}$ ranging from 5 to 100 $\mu$A, bias current $I_B$ set to 5, 20, 50 and 100 $\mu$A, and $V_{\text{DD}}$ set to 3.3 V. Moreover, the SCL transistors aspect ratios were sized as explained in Section 2.4, the buffer transistors’ aspect ratios were set to 0.6/0.3, 3/0.3 and 6/0.3, and the load capacitance, $C_L$, was set to 0 F, 50 fF, 200 fF and 1 pF. As an example, the resulting curves of the propagation delay predicted by Equation (15) and those simulated for $C_L = 200 \mu$F and $(W/L)_{\text{buf}} = 0.6/0.3$ are plotted in Figures 9(a)–9(d), where $I_B$ is set to 5, 20, 50 and 100 $\mu$A, respectively. As in Section 2.4, to get an idea about reasonable values used in practical cases, consider an SCL gate with $I_B = 20 \mu$A, $I_{\text{SF}} = 40 \mu$A, $C_L = 50 \mu$F, $(W/L)_a = 8/0.3$, $(W/L)_b = 0.6/0.7$, $(W/L)_{\text{buf}} = 3/0.3$ and $V_{\text{DD}} = 3.3$ V, whose predicted and simulated delay of 341 and 412 ps, respectively, differ by 17%.

The model agrees well with simulated results. Indeed, among the cases considered, the worst accuracy of 35% was found for $C_L = 200 \mu$F, $I_B = 5 \mu$A and $I_{\text{SF}} = 100 \mu$A. For other load and bias conditions error found is always lower, and for realistic values of bias currents, $I_B$ and $I_{\text{SF}}$, that lead to similar delay values for the internal SCL gate and the output buffer, the error is always lower than 20%, and usually is much lower. Indeed, the average error for $(W/L)_{\text{buf}}$ equal to 0.6/0.3, 3/0.3 and 6/0.3 is 14.7, 11.3 and 12.6%, respectively.

4. CONCLUSIONS

In this paper, an approach for the modelling of static and dynamic parameters of SCL gates with and without output buffer is proposed. In particular, logic swing, small-signal voltage
gain, noise margin and propagation delay are expressed as a function of design parameters and process data, according to the standard BSIM3v3 model of submicron MOS transistors.

The propagation delay model of a single SCL gate is based on a proper linearization of the circuit and the assumption of single-pole behaviour, first applying a step input. Moreover, for the circuits analysed, the transcapacitance model used to describe today’s CMOS devices dynamic behaviour is simplified into a model based on traditional self-capacitances, that is more suitable for circuit analysis.
To extend the analysis to cascaded SCL gates, the effect of the input rise time on the delay is also discussed, and it is shown that it can be neglected. Thus, the model developed for step input can also be used for actual input waveforms. Moreover, the loading effect of an SCL gate on the previous one is evaluated as a simple linear capacitance.

The model expressions are simple, thus they can be used for pencil-and-paper calculations and allow the designer to acquire an intuitive understanding of how performance depends on design parameters and technology. Hence, the model is useful right from the early design phases for first transistor and bias currents sizing, avoiding tedious trial-and-error design based on simulations.

The model’s validity has been tested by comparison with simulated results under many load and bias conditions, using a 0.35-μm CMOS process. The model has been found to be sufficiently accurate since the results predicted agree well with the simulated ones: in realistic cases, the difference is lower than 20% both for static parameters and delay. Therefore, the model proposed can be profitably used both for pencil-and-paper evaluations and for computer-based timing analysis of complex SCL circuits.

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The ratio $I_{D\text{SAT0}}/V_{SD}$ in Section 2.1 can be evaluated by considering the expression of current $I_{D\text{SAT0}}$ valid for both NMOS and PMOS transistors working in the linear region [27]:

$$I_{D\text{SAT0}} = \mu_{\text{eff}} C_{OX} \frac{W_{\text{eff}}}{L_{\text{eff}}} \left( |V_{GS}| - |V_{T}| - A_{\text{bulk}} \frac{|V_{DS}|}{2} \right) |V_{DS}|$$

(A1)

whose parameters are reported in the following with the subscript $p$ if referred to a PMOS transistor, and subscript $n$ in the case of an NMOS transistor.

In Equation (A1), parameters $W_{\text{eff}}$ and $L_{\text{eff}}$ are the effective channel width and length, $C_{OX}$ is the oxide capacitance per area, $V_{T}$ is the threshold voltage, $V_{GS}$ and $V_{DS}$ are the source–gate and source–drain voltages, and $\mu_{\text{eff}}$ is the effective carrier mobility defined as

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + (U_A + U_C|V_{SB}|)(|V_{GS}| + |V_{T}|/T_{OX}) + U_B(|V_{GS}| + |V_{T}|/T_{OX})^2} \frac{1}{1 + |V_{DS}|/E_{\text{SAT}} L_{\text{eff}}}$$

(A2)

where $E_{\text{SAT}}$ is the critical electric field at which carrier velocity becomes saturated, $U_A$, $U_B$ and $U_C$ are model parameters, and $T_{OX}$ is oxide thickness. It is worth noting that, in the denominator of (A2), the terms including $V_{GS}$ model the mobility degradation due to the vertical electric field in the MOS transistor, while those including $V_{DS}$ model the carrier velocity saturation due to the lateral electric field.

Parameter $A_{\text{bulk}}$ in Equation (A1) is slightly greater than the unity and is given by

$$A_{\text{bulk}} = \frac{1}{1 + K_{\text{ETA}}|V_{SB}|} \left\{ 1 + \frac{K_{10X}}{2\sqrt{\phi_S} - |V_{SB}|} \left[ \frac{A_0 L_{\text{eff}}}{L_{\text{eff}} + 2\sqrt{X_{JX_{\text{dep}}}}} \right] \right. \right. \left. \left. \times \left( 1 - A_{GS} (|V_{GS}| - |V_{T}|) \left( \frac{L_{\text{eff}}}{L_{\text{eff}} + 2\sqrt{X_{JX_{\text{dep}}}}} \right)^2 + \frac{B_0}{W_{\text{eff}} + B_1} \right) \right\}$$

(A3)

which depends on $W_{\text{eff}}$, $L_{\text{eff}}$ and various other BSIM3v3 model parameters. Function $A_{\text{bulk}}$ can be simplified by considering its maximum value, $A_{\text{bulk},\text{max}}$. This can be obtained by setting $W_{\text{eff}}$ to its minimum value and maximizing the resulting function with respect to $L_{\text{eff}}$, with straightforward calculations. As an example, for the PMOS transistor in a 0.35-μm CMOS process and $V_{DD} = 3.3$ V we get $A_{\text{bulk},\text{max},p} = 1.34$.

In particular, consider the active load PMOS transistor of the SCL gate, for which we have to set $V_{SG} = V_{DD}$ and source-bulk voltage, $V_{SB}$, equal to zero in Equations (A1) and (A2), and also $A_{\text{bulk},p} \approx A_{\text{bulk},\text{max},p} = 1.34$. Furthermore, since typical values of $\Delta V$ are much lower than $V_{DD} - |V_{T,p}|$, and $V_{SD}$ is small for the PMOS transistors, the terms $A_{\text{bulk},p} V_{SD}/2$ and $V_{SD}/E_{\text{SAT},p} L_{\text{eff},p}$ can be neglected in Equations (A1) and (A2). Therefore Equation (A1) becomes

$$I_{D\text{SAT0}} = \frac{V_{SD}}{R_{\text{int}}}$$

(A4)
where we have defined
\[ R_{\text{int}} = \left[ \mu_{\text{eff},p} C_{\text{OX}} \frac{W_{\text{eff},p}}{L_{\text{eff},p}} (V_{\text{DD}} - |V_{T,p}|) \right]^{-1} \]  
which represents the ‘intrinsic’ resistance of the PMOS transistor in the triode region, since it expresses the behaviour of the MOS transistor in the triode region without accounting for the parasitic drain/source resistance.

**APPENDIX B**

The noise margin of an SCL gate can be obtained from the expression of currents \( i_{D1} \) and \( i_{D2} \) as functions of input voltage \( v_i \) assuming transistor operation in the saturation region [33]:

\[
i_{D1}(v_i) = \begin{cases} 
0 & \text{if } v_i < -\sqrt{\frac{2I_B}{\mu_n C_{\text{OX}}(W/L)_{1,2}}} \\
\frac{I_B}{2} + \frac{v_i}{2} \sqrt{\mu_n C_{\text{OX}} \left( \frac{W}{L} \right)_{1,2} I_B - \left( \mu_n C_{\text{OX}} \left( \frac{W}{L} \right)_{1,2} \frac{v_i}{2} \right)^2} & \text{if } |v_i| \leq \sqrt{\frac{2I_B}{\mu_n C_{\text{OX}}(W/L)_{1,2}}} \\
I_B & \text{if } v_i > \sqrt{\frac{2I_B}{\mu_n C_{\text{OX}}(W/L)_{1,2}}} 
\end{cases}
\]

\( i_{D2}(v_i) = I_B - i_{D1}(v_i) \)  

Therefore, the output voltage can be expressed as

\[
v_o(v_i) = \begin{cases} 
\Delta V & \text{if } v_i < -\sqrt{\frac{2I_B}{\mu_n C_{\text{OX}}(W/L)_{1,2}}} \\
-\frac{v_i \Delta V}{I_B} \sqrt{\frac{\mu_{\text{eff},n} C_{\text{OX}}}{I_B} \frac{W_{\text{eff},n}}{L_{\text{eff},n}} \left( \frac{\mu_{\text{eff},n} C_{\text{OX}}}{2I_B} \frac{W_{\text{eff},n}}{L_{\text{eff},n} v_i} \right)^2} & \text{if } |v_i| \leq \sqrt{\frac{2I_B}{\mu_n C_{\text{OX}}(W/L)_{1,2}}} \\
-\Delta V & \text{if } v_i > \sqrt{\frac{2I_B}{\mu_n C_{\text{OX}}(W/L)_{1,2}}} 
\end{cases}
\]

whose typical trend is plotted versus input voltage, \( v_i \), in Figure B1. It is worth noting that Equation (B3) is symmetrical with respect to zero.

The noise margin is defined as \( V_{\text{OHmin}} - V_{\text{ILmin}} \) (or, equivalently, as \( V_{\text{ILmax}} - V_{\text{OLmax}} \), due to the symmetry with respect to zero), where \( V_{\text{ILmax}} \) and \( V_{\text{ILmin}} \) are the input voltage values such that \( \partial v_o / \partial v_i = -1 \), while \( V_{\text{OLmax}} \) and \( V_{\text{OHmin}} \) are the corresponding output voltages.
Figure B1. Typical trend of output voltage $v_o$ versus input voltage $v_i$ in an SCL inverter.

(i.e. $V_{OL\max} = v_o(V_{IH\min})$ and $V_{OH\min} = v_o(V_{IL\max})$), as shown in Figure B1. By differentiating Equation (B3) with respect to $v_i$ and setting it to $-1$, $V_{IH\min}$ results to

$$V_{IH\min} = \sqrt{\frac{2I_B}{\mu_{eff,n}C_{OX}W_{eff,n}/L_{eff,n}}} - \frac{I_B}{2\mu_{eff,n}C_{OX}W_{eff,n}/L_{eff,n}} \frac{1}{AV} \left(\sqrt{1 + 8AV^2} + 1\right)$$

$$\approx \sqrt{\frac{2I_B}{\mu_{eff,n}C_{OX}W_{eff,n}/L_{eff,n}}} \left(1 - \frac{1}{\sqrt{2}AV}\right)$$  \hspace{1cm} (B4)

where Equation (6) was used and $AV \gg 1/\sqrt{8}$ was assumed. Approximating $V_{OH\min}$ to $\Delta V$ leads to the following expression of noise margin:

$$NM = \Delta V \left(1 - \frac{\sqrt{2}}{AV} \sqrt{1 - \frac{1}{\sqrt{2}AV}}\right) \approx \Delta V \left(1 - \frac{\sqrt{2}}{AV}\right)$$  \hspace{1cm} (B5)

where $AV \gg 1/\sqrt{2}$ was assumed.

REFERENCES